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Layout Design Rule

For EXC80H80, EXC80H100 & EXC82H100



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EDG-025-180105-1	2018/01/05	Reorganize figures orders.
EDG-025-180622-1	2018/06/22	Add EXC82H100 layout design rule
EDG-025-180910-1	2018/09/10	Fix watermark.

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1 Introduction

The purpose of this design guideline is to optimize the layout of EXC80H & EXC82H printed circuit board (PCB) which the layout engineers should follow as a reference.

1. EXC80H80 & EXC80H100

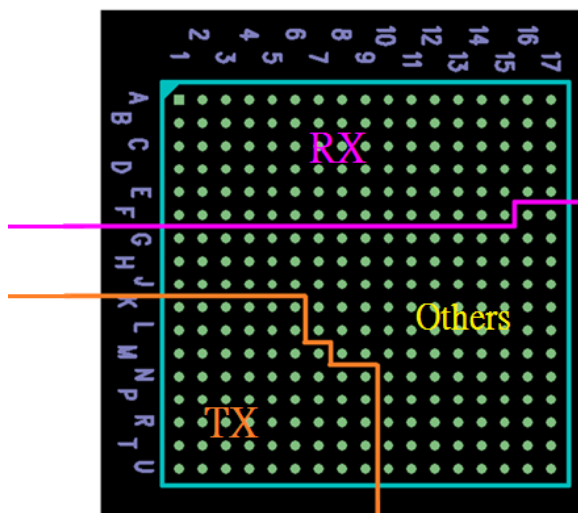


Figure 1. EXC80H IC pin-out

2. EXC82H100

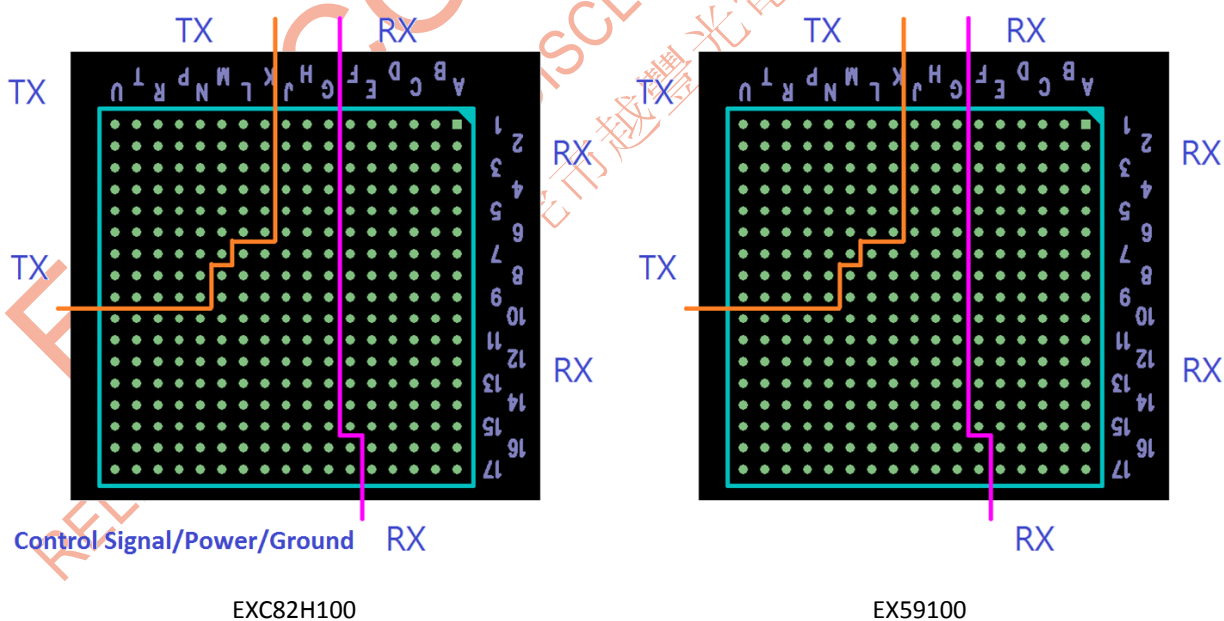


Figure 2. EXC82H IC pin-out for master (EXC82H100) & slave chip (EX59100)

2 IC Discrete Circuit

The resistors & capacitors on the following circuits must be placed closely to the chip.

Depends on the requirement, the test points could be placed on either sides of the PCB.

2.1 EXC80H80 & EXC80H100

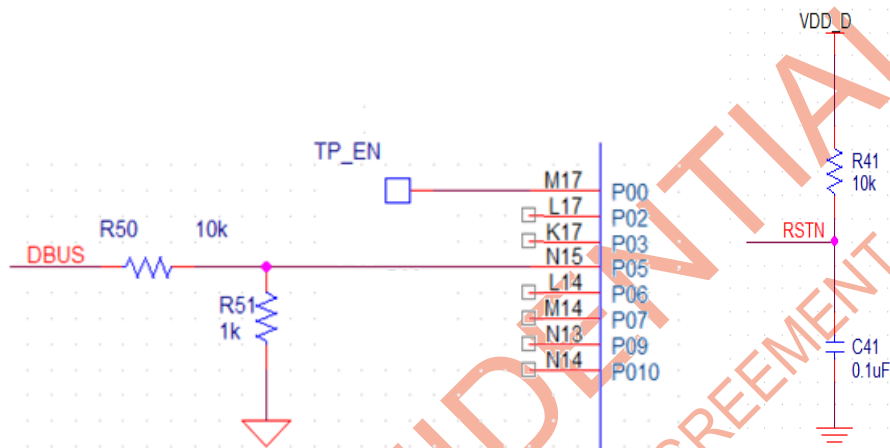


Figure 3. EXC80H80 & EXC80H100 discrete circuit-1

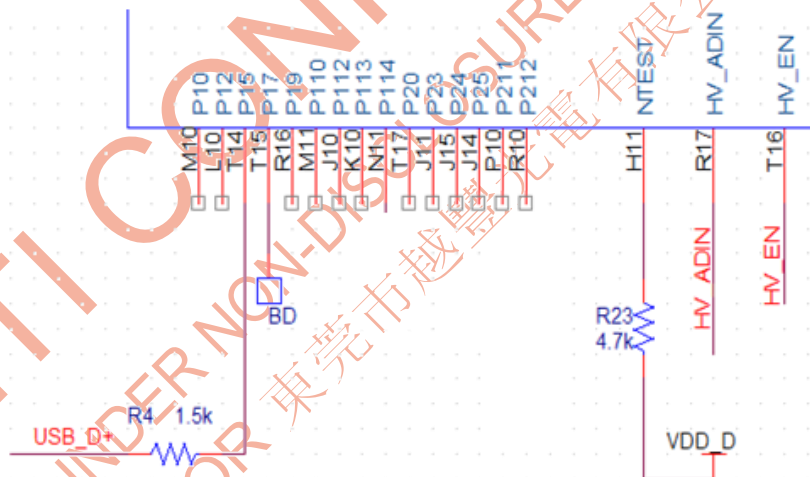


Figure 4. EXC80H80 & EXC80H100 discrete circuit-2

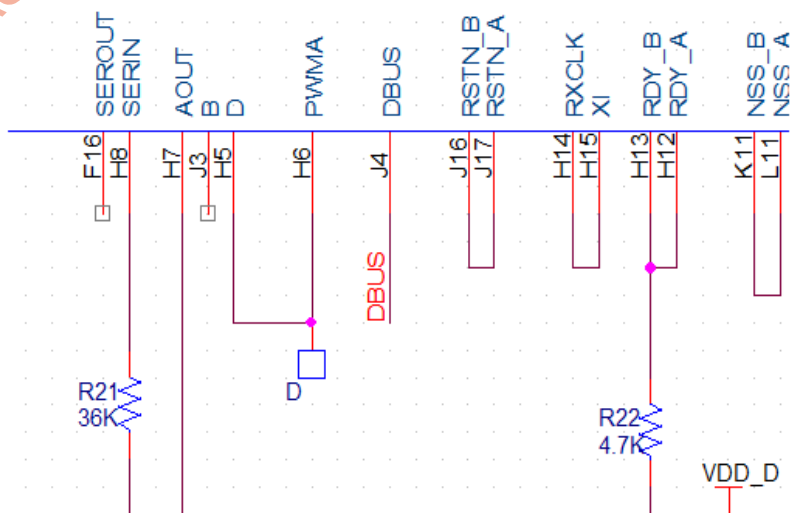


Figure 5. EXC80H80 & EXC80H100 discrete circuit-3

2.2 EXC82H100

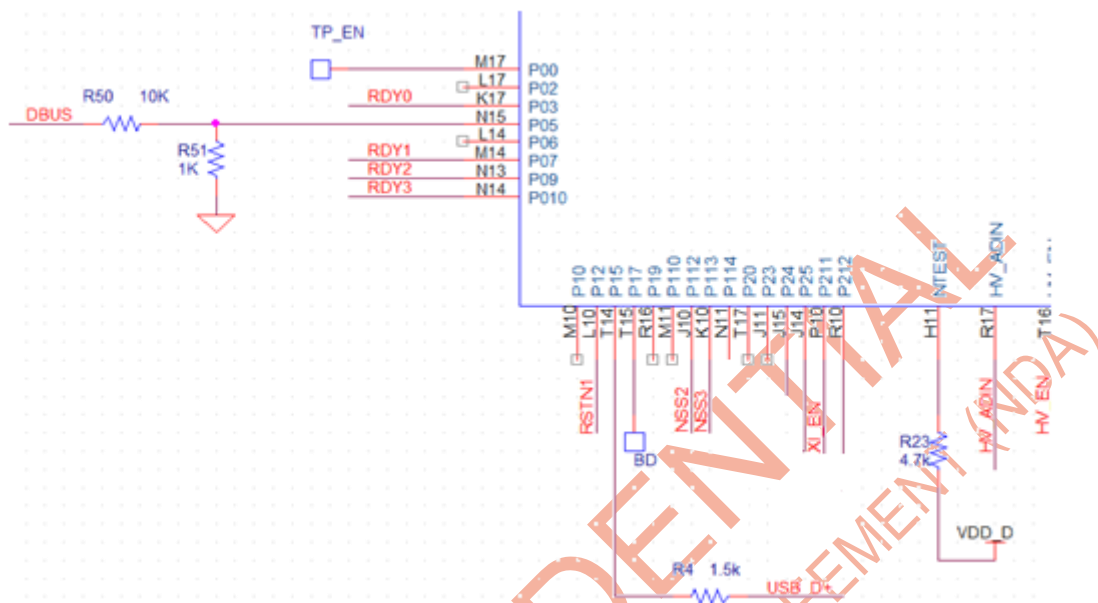


Figure 6. EXC82H100 discrete circuit-1

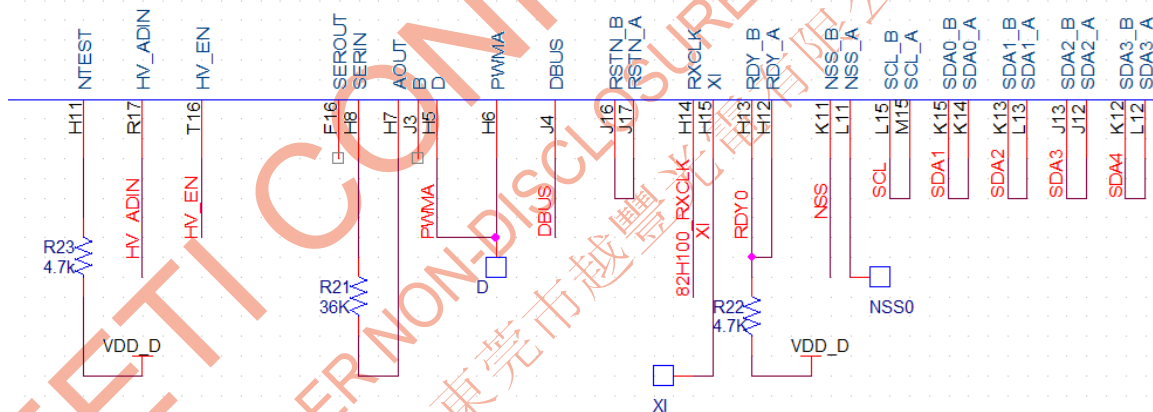


Figure 7. EXC82H100 discrete circuit-2

The connection from PWMA, RXCLK, XI, SCL & SDA1-SDA4 to other components can go through the power layer. However, SCL & SDA1-SDA4 must place together.

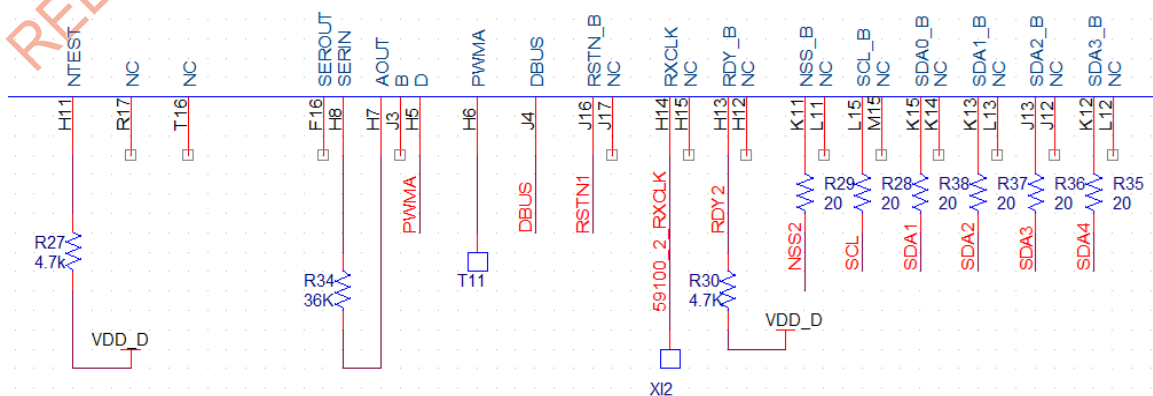


Figure 8. EXC82H100 discrete circuit-3

3 Transient Voltage Suppressor

The Transient Voltage Suppressor (TVS) has to be placed close to the input connector of communication signal; all input communication must go through the TVS first before entering into other components. Please refer to the following flow chart & schematic for proper TVS connection design.

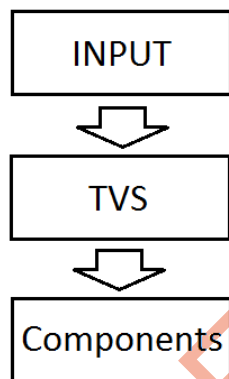


Figure 9. TVS flow chart

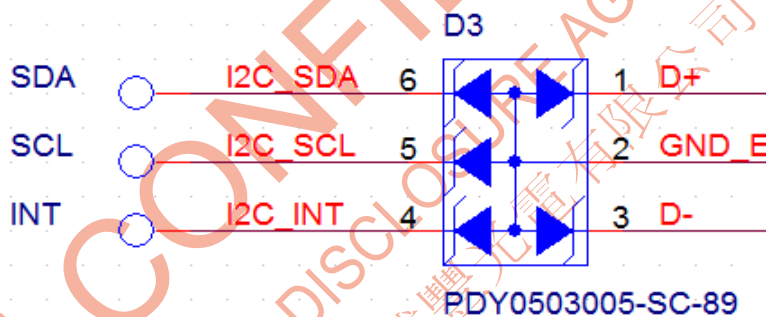
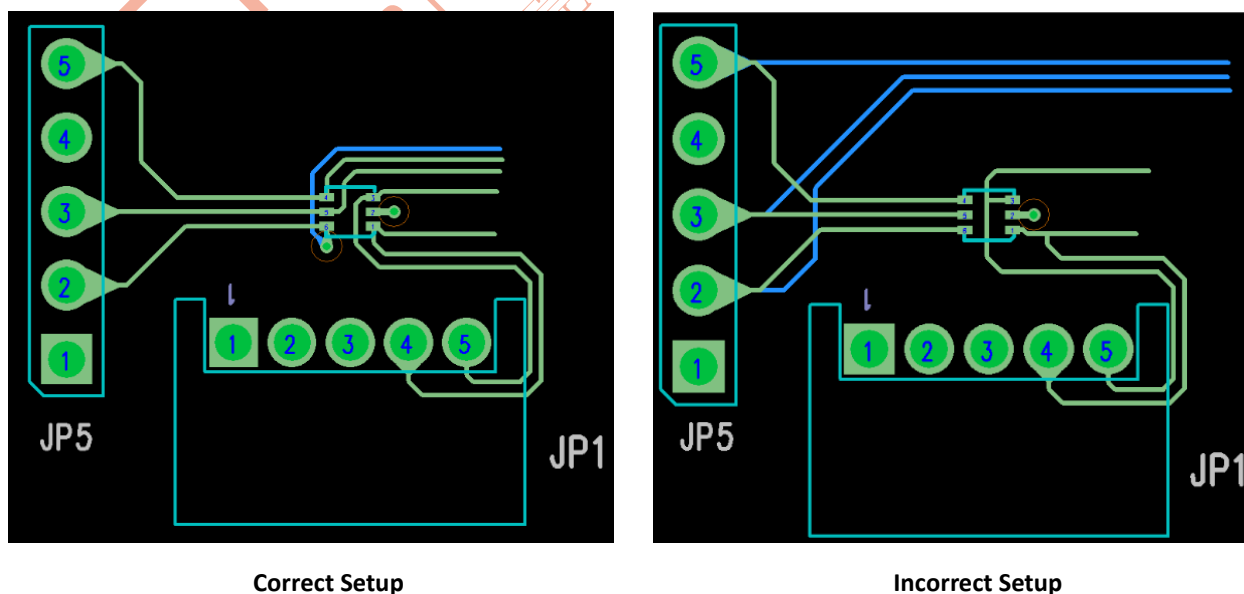


Figure 10. TVS schematic



Correct Setup

Incorrect Setup

Figure 11. TVS layout examples

4 USB Communication Circuit

The components in figure 12 must be placed close to the connector. The 5 pin connector is for reference only. L1, L2, R13, R14 have to be placed near the input connector and the TVS. Vertical Interconnect Access (VIA) is allowed to use on the signal D+/D- with shortest path but USB_D+/USB_D- are not and have to go with 6 mil traces.

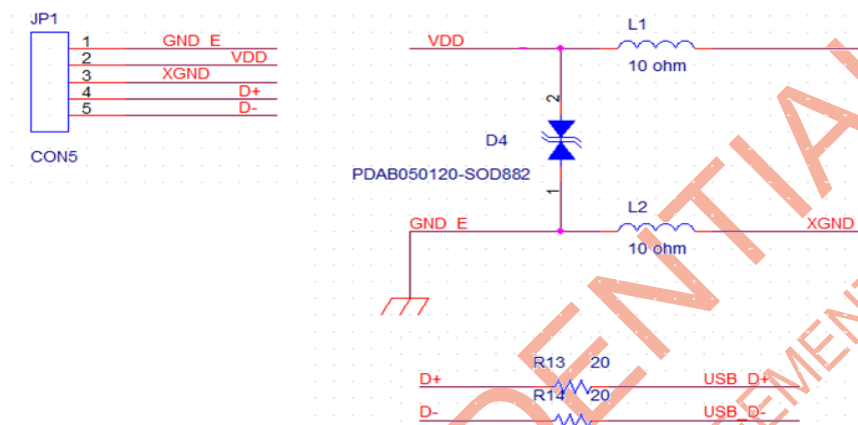


Figure 12. USB Communication Circuit

5 RS232 Communication Circuit

The components in figure 13 & 14 must be placed close to the connector.

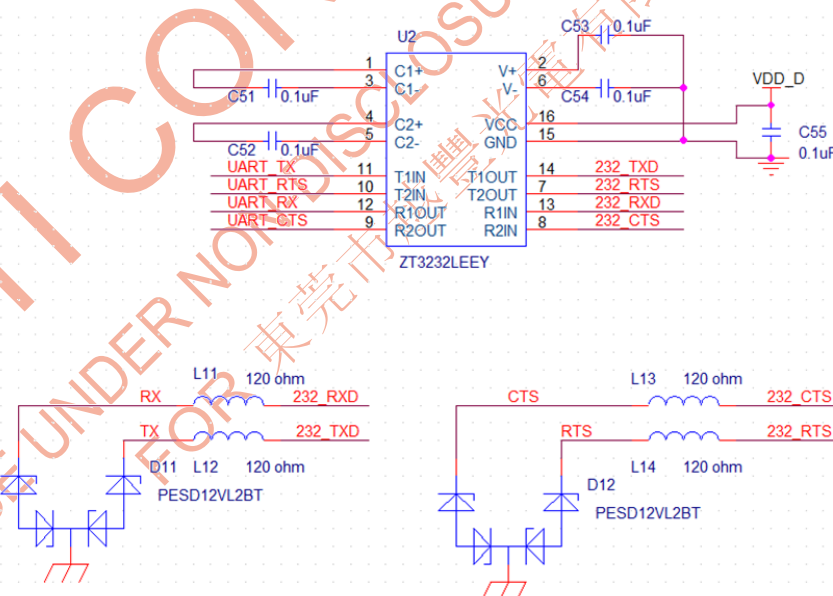


Figure 13. RS232 Communication Circuit-1

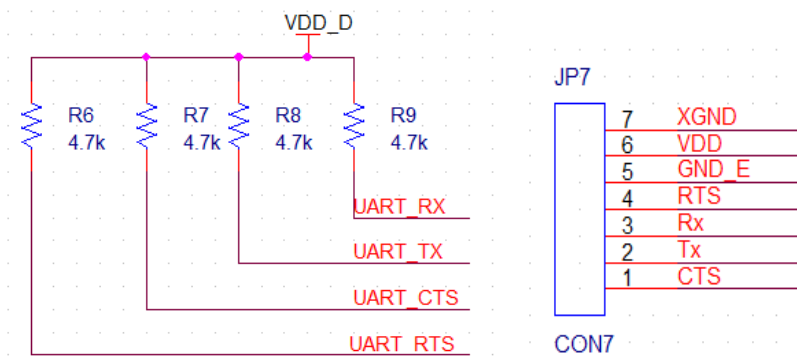


Figure 14. RS232 Communication Circuit-2

6 Low Dropout Linear Regulator & Buck

6.1 EXC80H80 & EXC80H100

The discrete components in figure 15 must be placed near the LDO (U1) and use VIA as less as possible. All the power sources/grounds must go through C4, C5 and C30 before entering into other components such as capacitors and resistors (Use VIA through C4, C5 and C30).

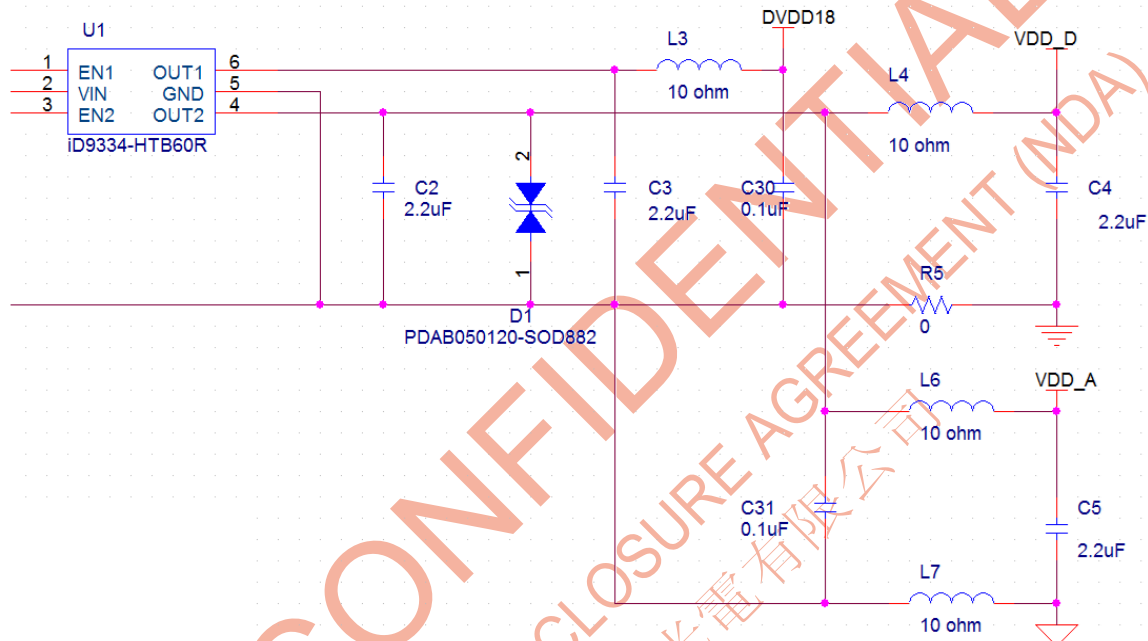


Figure 15. EXC80H80 & EXC80H100 Low Dropout Linear Regulator Circuit

6.2 EXC82H100

For EXC82H, it is the same as EXC80H in section 6.1. However, for the buck circuit, please follow the layout consideration in U6's data sheet.

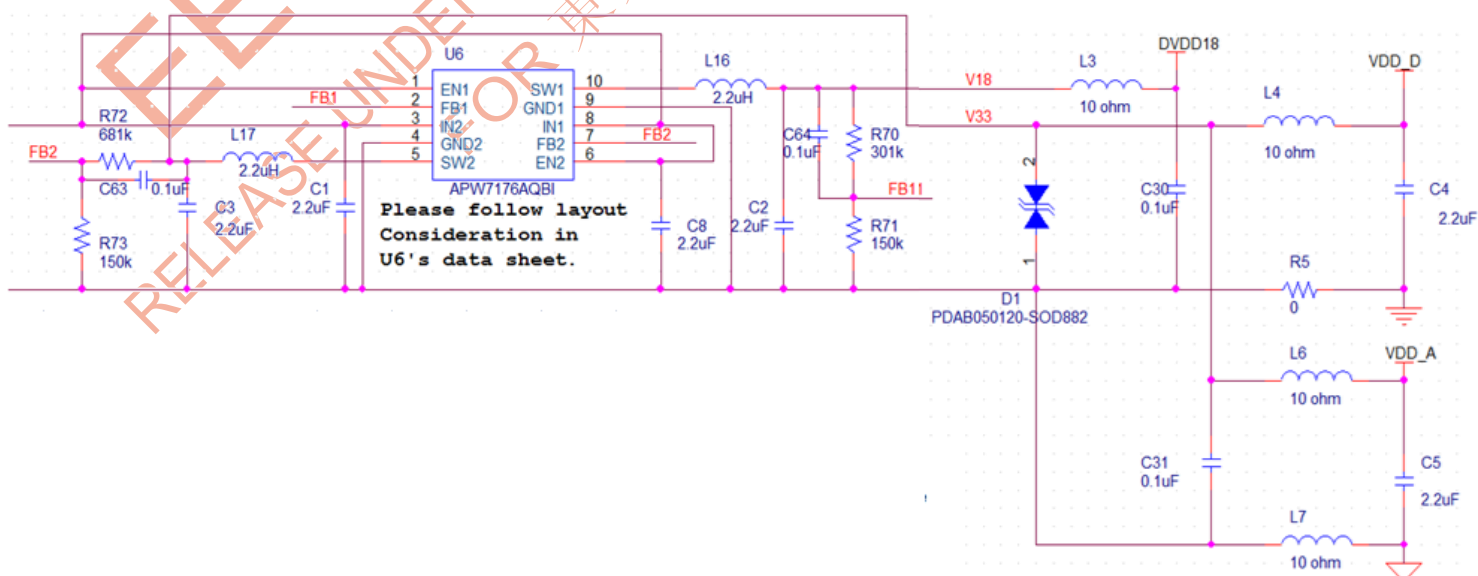


Figure 16. EXC82H100 Buck Circuit

7 High-Voltage Boost Circuit

The components in figure 17 must be placed near U3 with shortest path and use VIA as less as possible. All the power sources/grounds are connected from C11 to the rest of the components such as capacitors and resistors (Use VIA through C11). Place VDDH close to the IC with shortest path.

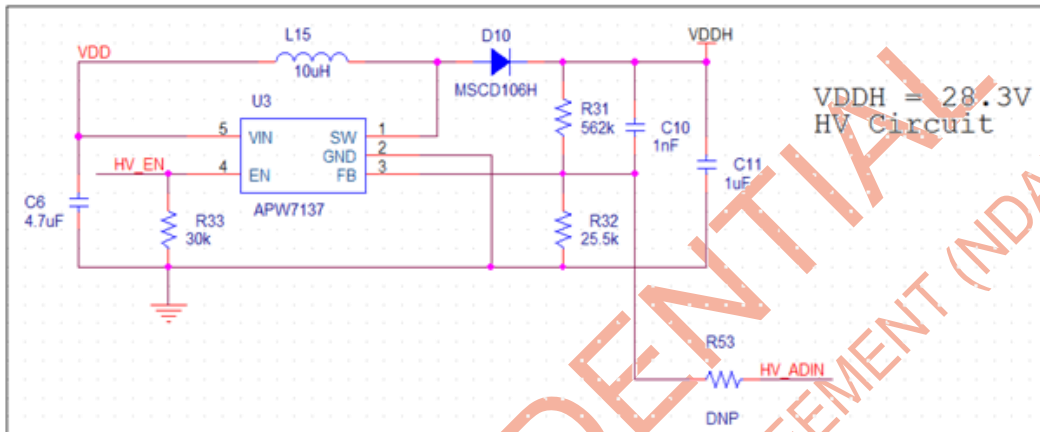


Figure 17. High-Voltage Boost Circuit

8 By Pass Capacitors

All of the bypass capacitors have to be placed near the chips with shortest path. All chips must connect to the capacitors first before entering into power sources/grounds.

9 Test Points

Test points must be organized and placed together when spaces are available.

Figure 18 is an example of how the test points should be laid out.

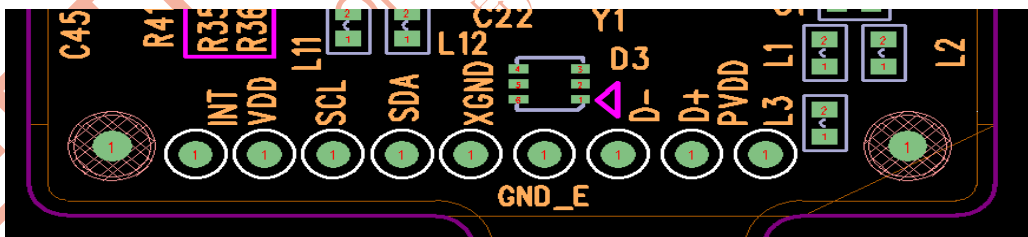


Figure 18. Test Points

Figure 19 is an example of how to place the test points with a connector

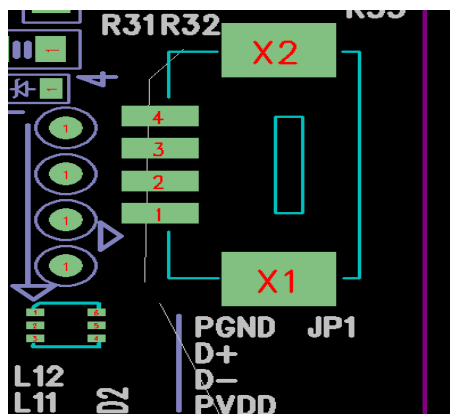


Figure 19. Example of test points layout

10 E-type Active Stylus

If the E-type active stylus is required, L8 & D8 in the circuit below must be placed near the connector. Keep the signal TX_Pen within a single layer. Please note, the trace of TX_Pen can't go parallel with TX channels while layout and keep a gap of at least 5 channels away from next valid TX channel.

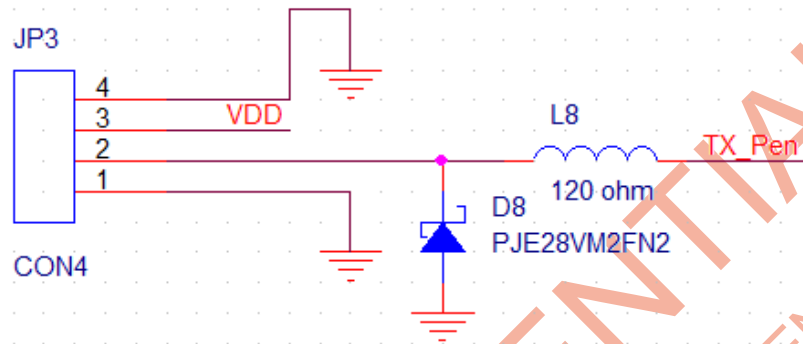


Figure 20. E-type Active Stylus Discrete Circuit

11 Trace Design

The traces from bonding pad to the IC have to be kept at the same width and gap, same as the Flexible Printed Circuit (FPC) cable. The following figure shows the layout when the spaces are available. Vertical Interconnect Access (VIA) are close to the IC

11.1 EXC80H80 & EXC80H100

The following figure shows the layout when the spaces are not available. Vertical Interconnect Access (VIA) are close to the connector.

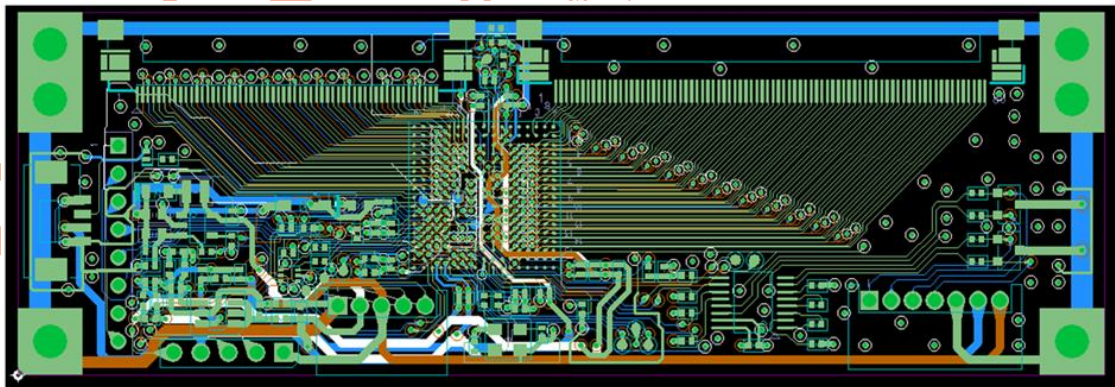


Figure 21. Trace design when space is not available

11.2 EXC82H100

The TX & RX channels do have orders. When laying the trace, please follow the channel orders. If VIAs are required, make sure the traces are within the same layer and keep it organized as FPC.

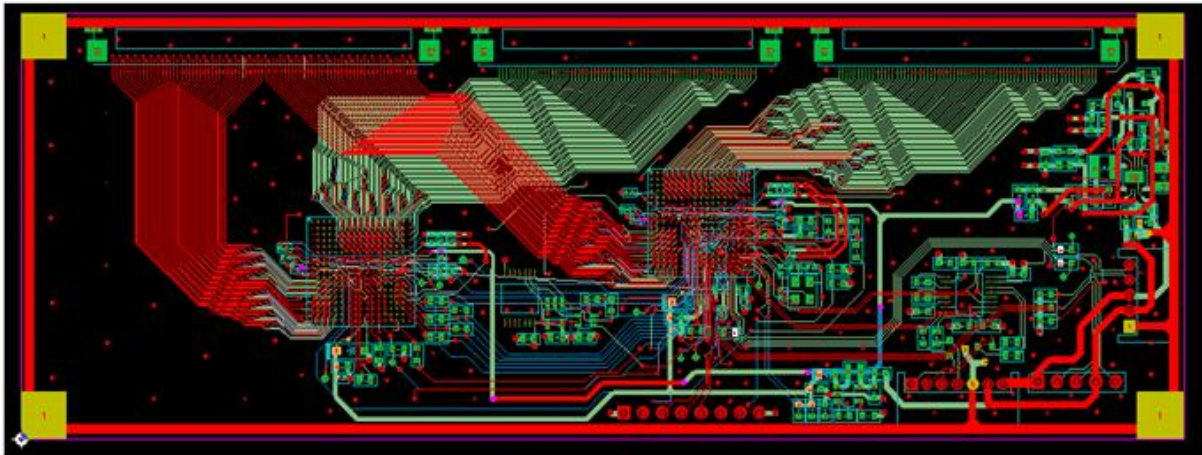


Figure 22. Trace design

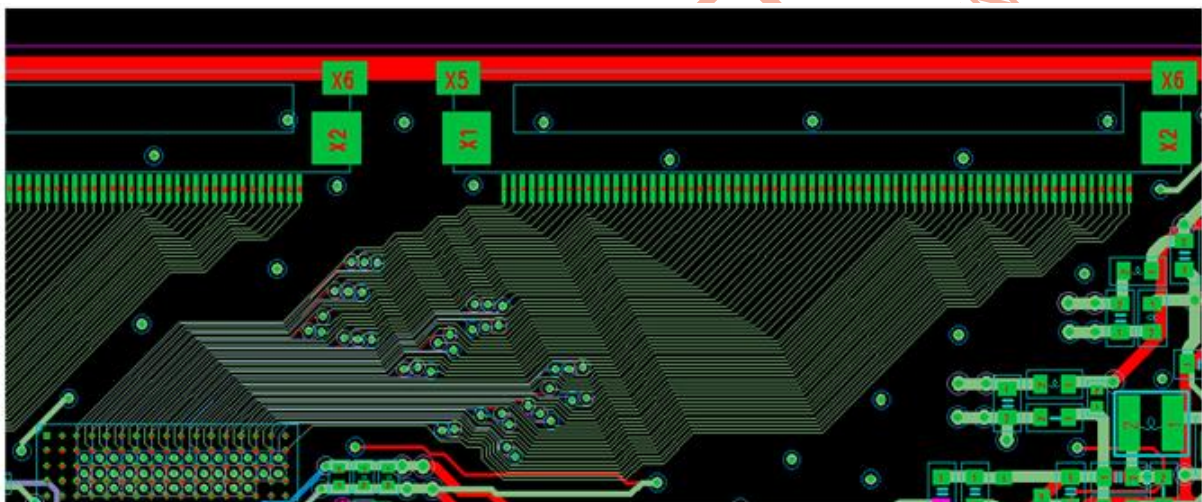


Figure 23. PCB design zoomed in 1

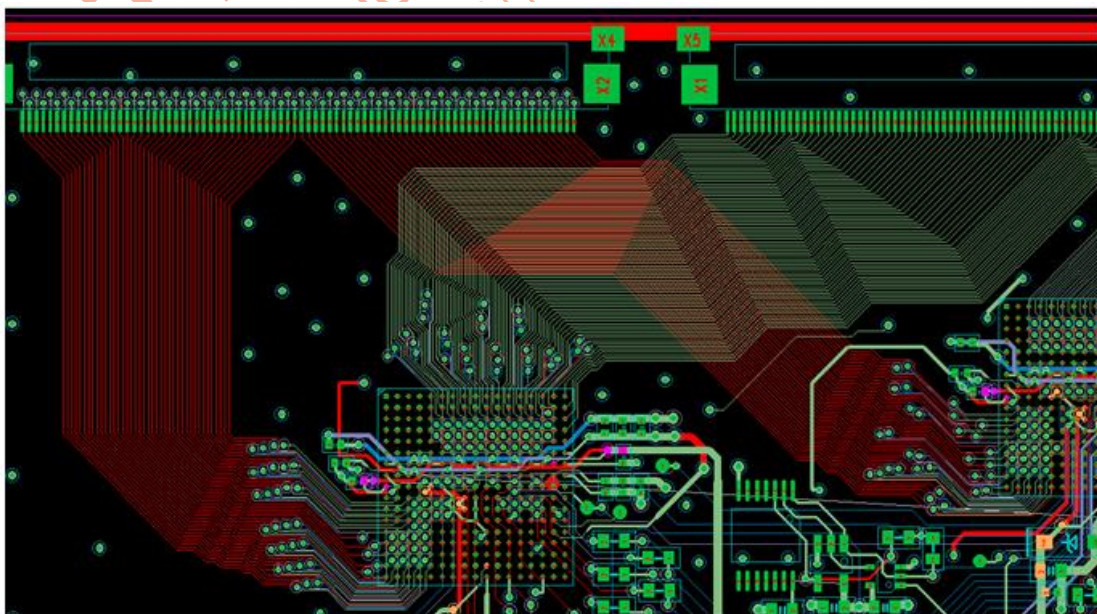


Figure 24. PCB design zoomed 2

12 Overall Layout

12.1 EXC80H80 & EXC80H100

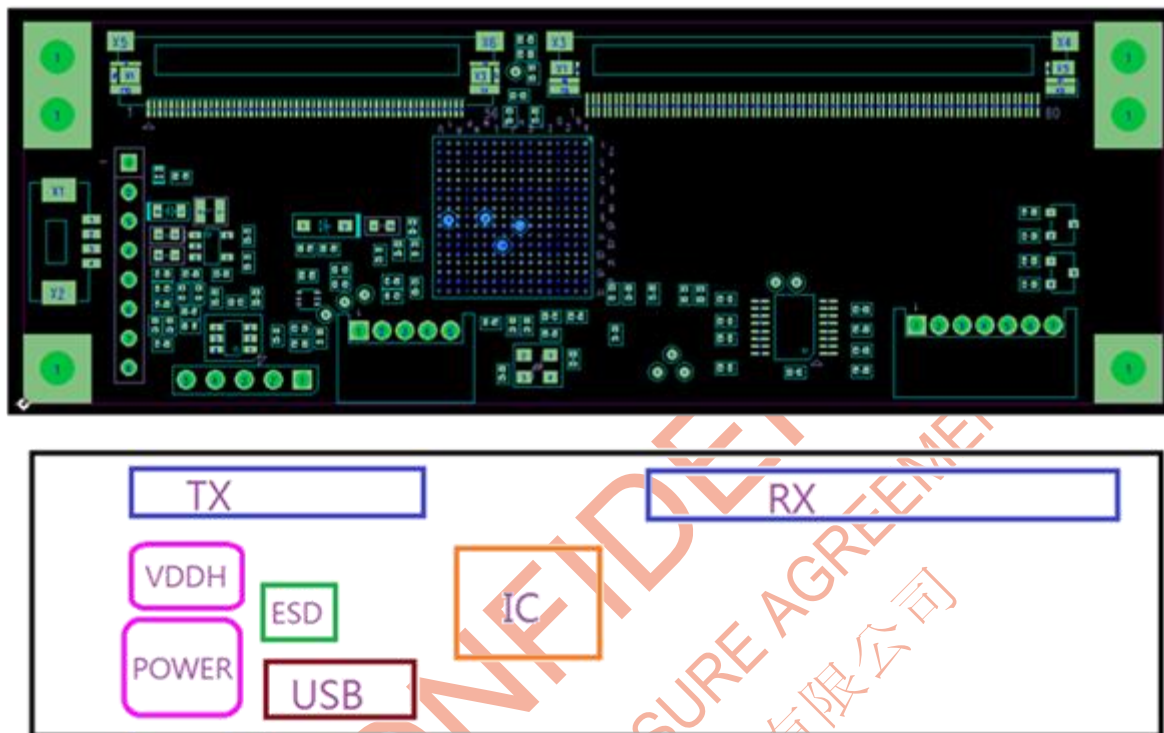


Figure 25. EXC80H80 & EXC80H100 Overall Layout

12.2 EXC82H100

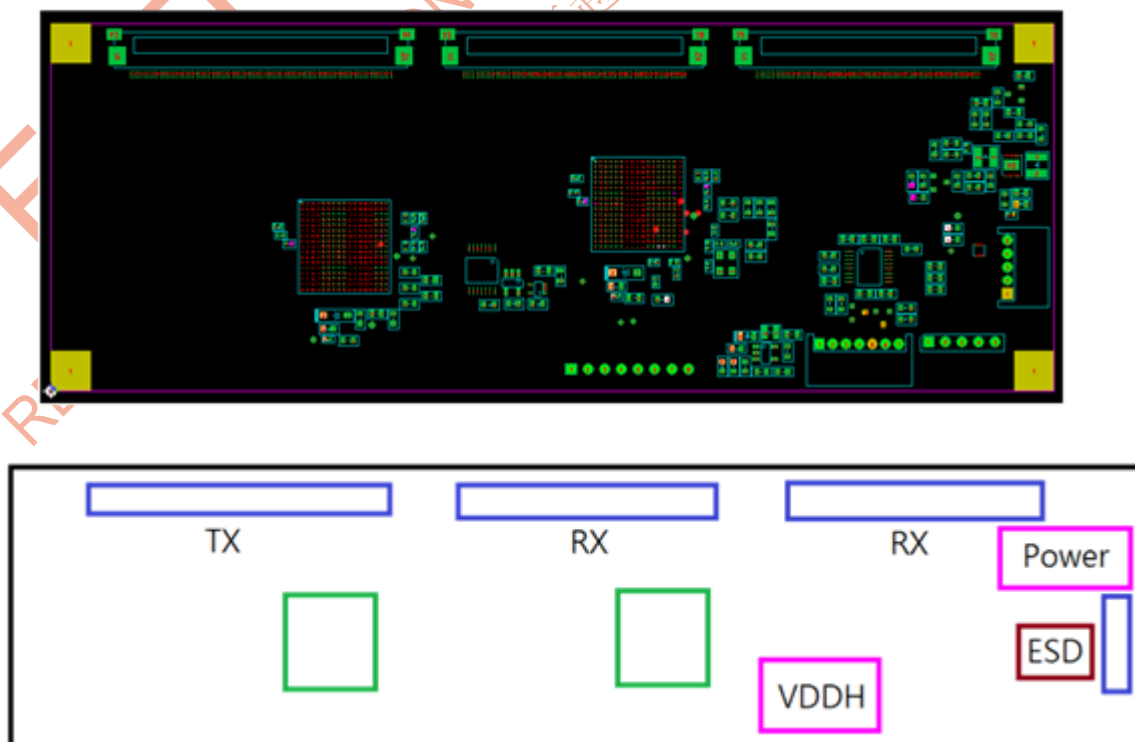


Figure 26. EXC82H100 Overall Layout

	Signal	Trace Width		Remark
		Min	Typical	
I2C	I2C_SDA,I2C_SCL,I2C_INT	4	6	Place these 3 signals together
Channel X/Y	Tx/Rx	4	4	Same width and gap
USB	USB D+/D-	4	6	It is recommend to add GND as shielding, keep it parallel and away from other signals
	VDD/GND		12 ~ 15	
	USB_EN	4	6	Power and ground. Trace width at starting point can be 15mil and ending point can be 12mil. Check the layout from IC to BY PASS
POWER	VDD_D/GND	12 or 15	12 ~ 20	FR4 Board power trace is about 25~40mil
XTAL	XIN , XOUT	8	10	

Table 1

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